Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

Claims 1-105 (canceled)

106. (currently amended) A semiconductor chip or wafer comprising:

a silicon substrate;

a metallization structure over said silicon substrate;

a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a first contact pad of said metallization structure, and wherein said passivation layer comprises an inorganic material; ~~and~~

a polymer layer over said passivation layer, wherein said polymer layer has a thickness of between 2 and 50 μm; and

a metal trace over part of said polymer ~~passivation~~ layer and over said first contact pad, wherein said metal trace comprises a gold layer with a thickness of between 2 and 100 μm, and wherein said metal trace comprises a second contact pad connected to said first contact pad, ~~and~~ wherein the positions of said first and second contact pads from a top perspective view are different.

107. (previously presented) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip or wafer.

108. (previously presented) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

109. (previously presented) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost CVD-formed layer of said semiconductor chip or wafer.

110. (previously presented) The semiconductor chip or wafer of claim 106, wherein said metal trace further comprises a titanium-containing layer under said gold layer.

Claim 111 (canceled)

112. (previously presented) The semiconductor chip or wafer of claim 106, wherein said second contact pad is used to be wirebonded thereto.

113. (previously presented) The semiconductor chip or wafer of claim 106 further comprising a wirebond over said second contact pad.

114. (previously presented) The semiconductor chip or wafer of claim 106 further comprising a metal bump over said second contact pad.

115. (previously presented) The semiconductor chip or wafer of claim 106 further comprising a solder bump over said second contact pad.

116. (currently amended) The semiconductor chip or wafer of claim 106, wherein no polymer layer is over said metal trace. ~~further comprising a topmost polymer layer over said passivation layer, wherein said metal trace is over said topmost polymer layer.~~

Claims 117-118 (canceled)

119. (previously presented) The semiconductor chip or wafer of claim 106, wherein said gold layer is electroplated.

120. (previously presented) A semiconductor chip or wafer comprising:

a silicon substrate;

a metallization structure over said silicon substrate;

a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a first contact pad of said metallization structure, and wherein said passivation layer comprises an inorganic material; and

a second contact pad connected to said first contact pad, wherein said second contact pad comprises a gold layer with a thickness of between 2 and 15 μm and is used to be wirebonded thereto.

Claims 121 and 122 (canceled)

123. (previously presented) The semiconductor chip or wafer of claim 120 further comprising a polymer layer over said passivation layer, wherein said second contact pad is over said polymer layer.

Claims 124 and 125 (canceled)

126. (previously presented) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip or wafer.

127. (previously presented) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

128. (previously presented) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost CVD-formed layer of said semiconductor chip or wafer.

129. (previously presented) The semiconductor chip or wafer of claim 120, wherein said gold layer is electroplated.

Claim 130 (canceled)

131. (previously presented) The semiconductor chip or wafer of claim 120 further comprising a wirebond over said second contact pad.

Claims 132-135 (canceled)

136. (currently amended) A circuit ~~circuitry~~ component comprising:

a semiconductor substrate;

a metallization structure over said semiconductor substrate;

a passivation layer over said metallization structure, ~~wherein said metallization structure comprises a first pad exposed by an opening in said passivation layer, and~~ wherein said passivation layer comprises an inorganic material; and

a metal trace over said passivation layer, wherein said metal trace comprises a titanium-containing layer, a first gold layer on said titanium-containing layer, and a second gold layer on said first gold layer, wherein said titanium-containing layer has a thickness of between 0.01 and 3 μm, said first gold layer has a thickness of between 0.05 and 3 μm, and a said second gold layer ~~with~~ has a thickness of between 2 and 100 μm.

137. (currently amended) The circuit ~~circuitry~~ component of claim 136, wherein said metal trace comprises a pad used to be wirebonded thereto.

138. (currently amended) The circuit ~~circuitry~~ component of claim 136, wherein said metal trace comprises a pad used to have a metal bump formed thereon.

139. (currently amended) The circuit ~~circuitry~~ component of claim 136 further comprising a polymer layer between said metal trace and said passivation layer. ~~, wherein said metal trace comprises a titanium-containing layer under said gold layer.~~

140. (currently amended) The circuit ~~circuitry~~ component of claim 136, wherein said second gold layer is electroplated.

141. (new) The semiconductor chip or wafer of claim 110, wherein said titanium-containing layer has a thickness of between 0.01 and 3 μm.

142. (new) The semiconductor chip or wafer of claim 110, wherein said metal trace further comprises another gold layer between said titanium-containing layer and said gold layer, wherein said another gold layer has a thickness of between 0.05 and 3 μm.

143. (new) The semiconductor chip or wafer of claim 120, wherein said second contact pad further comprises a titanium-containing layer under said gold layer.

144. (new) The semiconductor chip or wafer of claim 143, wherein said titanium-containing layer has a thickness of between 0.01 and 3 μm.

145. (new) The semiconductor chip or wafer of claim 143, wherein said metal trace further comprises another gold layer between said titanium-containing layer and said gold layer, wherein said another gold layer has a thickness of between 0.05 and 3 μm.

146. (new) The semiconductor chip or wafer of claim 123, wherein said polymer layer has a thickness of between 2 and 50 μm.

147. (new) The circuit component of claim 139, wherein said polymer layer has a thickness of between 2 and 50 μm.

148. (new) The circuit component of claim 136, wherein said passivation layer comprises a topmost nitride layer of said circuit component.

149. (new) The circuit component of claim 136, wherein said passivation layer comprises a topmost oxide layer of said circuit component.

150. (new) The circuit component of claim 136, wherein said passivation layer comprises a topmost CVD-formed layer of said circuit component.

151. (new) The circuit component of claim 136, wherein no polymer layer is over said metal trace.